GP 2811

CERTIFICATE OF MAILING BY FIRST CLASS MAIL (37 CFR 1.8) Applicant(s): JACK H. LINN ET AL.			Docket No. 87552.99R134/SE-906D
Serial No. 09/316,580	Filing Date MAY 21, 1999	Examiner	Group Art Unit

Invention: BONDED WAFER PROCESSING WITH METAL SILICIDATION

I hereby certify that this **Power of Attorney**
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Docket No.
87552.97R017

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Title: **(See Attached Listing)**

Serial No., if Any: **(See Attached Listing)**
Filed: **(See Attached Listing)**

TO THE ASSISTANT COMMISSIONER FOR PATENTS

The Assistant Commissioner for Patents
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Dated: **October 5, 2000**

INTERSIL CORPORATION

SERIAL NO.	FILED DATE	TITLE
08/190,998	2/3/1994	METHOD FOR PROVIDING A SILICON AND DIAMOND SUBSTRATE HAVING A CARBON TO SILICON TRANSITION LAYER AND APPARATUS THEREOF
08/587,953	1/17/1996	METHOD FOR PROVIDING A SILICON AND DIAMOND SUBSTRATE HAVING A CARBON TO SILICON TRANSITION LAYER AND APPARATUS THEREOF
08/483,691	6/7/1995	HIGH EFFICIENCY POWER MOS SWITCH
08/613,381	3/7/1996	CIRCUIT FOR DRIVING AN ELECTROLUMINESCENT LAMP
08/483,692	6/7/1995	PILOT TRANSISTOR FOR QUASI-VERTICAL DMOS DEVICE
08/722,354	9/27/1996	SWITCHING AMPLIFIER CLOSED LOOP DUAL COMPARATOR MODULATION TECHNIQUE
08/269,470	6/30/1994	HIGH SPEED A/D CONVERTER AND SLEW CONTROLLED PULSE DETECTOR
08/666,258	6/20/1996	RADIATION HARDENED DIELECTRIC FOR EEPROM
09/061,602	4/16/1998	RADIATION HARDENED DIELECTRIC FOR EEPROM
08/673,396	6/28/1996	HIGH VOLTAGE PROTECTION CIRCUITS
08/474,559	6/7/1995	HIGH EFFICIENCY QUASI-VERTICAL DMOS IN CMOS OR BICMOS PROCESS
08/658,010	6/4/1996	INTEGRATED CIRCUIT AIR BRIDGE STRUCTURES AND METHODS OF FABRICATING SAME
09/199,292	11/24/1998	INTEGRATED CIRCUIT AIR BRIDGE STRUCTURES AND METHODS OF FABRICATING SAME
08/800,574	2/18/1997	NARROWBAND VIDEO CODEC
08/634,371	4/18/1996	ASYMMETRIC SNUBBER RESISTOR
08/636,904	4/16/1996	TRENCH MOS GATE DEVICE
09/096,217	6/11/1998	TRENCH MOS GATE DEVICE
08/462,171	6/5/1995	SURFACE MOUNTABLE INTEGRATED CIRCUITS AND METHODS OF FABRICATION
08/505,671	7/21/1995	FAST RECOVERY TEMPERATURE COMPENSATED REFERENCE SOURCE
08/497,404	6/30/1995	SEMI-INSULATING WAFER
08/637,132	4/24/1996	INTEGRATED CIRCUIT WITH AN IMPROVED INDUCTOR STRUCTURE AND METHOD OF FABRICATION
08/650,762	5/20/1996	PRE-BOND CAVITY AIR BRIDGE
08/462,876	6/5/1995	SYSTEM FOR INTERCONNECTING STACKED INTEGRATED CIRCUITS
08/586,613	1/16/1996	METAL OXIDE SEMICONDUCTOR CONTROLLED THYRISTOR WITH AN ON-FIELD EFFECT TRANSISTOR IN A TRENCH
08/336,768	11/9/1994	METHOD FOR MAKING OHMIC CONTACT TO LIGHTLY DOPED ISLANDS FROM A SILICIDE BURIED LAYER AND APPLICATIONS
08/810,127	2/25/1997	METHOD FOR MAKING OHMIC CONTACT TO LIGHTLY DOPED ISLANDS FROM A SILICIDE BURIED LAYER AND APPLICATIONS
08/505,695	7/21/1995	AUTOMATIC FAULT MONITORING SYSTEM AND MOTOR CONTROL SYSTEM INCORPORATING SAME
08/461,951	6/5/1995	METHOD OF BONDING WAFERS HAVING VIAS INCLUDING CONDUCTIVE MATERIAL
08/461,037	6/5/1995	INTEGRATED CIRCUIT WITH COAXIAL INSOLATION AND METHOD
08/042,299	4/2/1993	DIAMOND INSULATOR DEVICES AND METHOD OF FABRICATION
08/471,759	6/6/1995	DIAMOND INSULATOR DEVICES AND METHOD OF FABRICATION
08/662,118	6/12/1996	METHOD FOR FABRICATING A POWER DEVICE AND APPARATUS THEREOF
09/330,437	6/11/1999	METHOD FOR FABRICATING A POWER DEVICE AND APPARATUS THEREOF
08/637,937	4/23/1996	PROCESS OF FORMING TRENCH ISOLATION DEVICE
09/283,530	4/1/1999	PROCESS OF FORMING TRENCH ISOLATION DEVICE
08,650,688	5/20,1996	INTEGRATED CIRCUIT WITH AN AIR BRIDGE HAVING A LID
08/771,944	12/23/1996	DEEP TRENCH ETCH ON BONDED SILICON WAFER
09/266,066	3/10/1999	DEEP TRENCH ETCH ON BONDED SILICON WAFER
08/481,115	6/7/1995	DEFECT CONTROL IN FORMATION OF DIELECTRICALLY ISOLATED SEMICONDUCTOR DEVICE REGIONS
07/939,786	9/3/1992	BONDED WAFER PROCESSING WITH METAL SILICIDATION
08/351,933	12/8/1994	BONDED WAFER PROCESSING WITH METAL SILICIDATION
08/915,841	8/21/1997	BONDED WAFER PROCESSING WITH METAL SILICIDATION
09/316,580	5/21/1999	BONDED WAFER PROCESSING WITH METAL SILICIDATION
08/973,769	7/27/1998	MONOLITHIC CLASS C AMPLIFIER
09/392,806	9/9/1999	MONOLITHIC CLASS C AMPLIFIER
08/646,471	5/8/1996	SEMICONDUCTOR DEVICE WITH DOPED SEMICONDUCTOR AND DIELECTRIC TRENCH SIDEWALL LAYERS
08/705,536	8/29/1996	LID WAFER BOND PACKAGING AND MICROMACHINING
09/073,776	5/6/1998	LID WAFER BOND PACKAGING AND MICROMACHINING
08/671,243	6/27/1996	INTEGRATED CIRCUIT CONTAINING DEVICES DIELECTRICALLY ISOLATED AND JUNCTION ISOLATED FROM SUBSTRATE
08/310,280	9/21/1994	PROGRAMMABLE ELEMENT IN BARRIER METAL DEVICE AND METHOD
08/586,556	1/16/1996	METHOD AND APPARATUS FOR RADIATION HARDENED ISOLATION

08/596,079	2/6/1996	ELECTROSTATIC DISCHARGE PROTECTION DEVICE
09/268,605	3/15/1999	ELECTROSTATIC DISCHARGE PROTECTION DEVICE
07/674,147	3/25/1991	GRADED COLLECTOR FOR INDUCTIVE LOADS
08/191,963	2/3/1994	GRADED COLLECTOR FOR INDUCTIVE LOADS
08/356,683	12/14/1994	HOME VIDEO CONFERENCING SYSTEM (HAS)
08/463,388	6/5/1995	INTEGRATED CIRCUIT WITH EDGE CONNECTIONS AND METHOD
08/481,116	6/7/1995	LOCAL OXIDATION PROCESS FOR HIGH FIELD THRESHOLD APPLICATIONS
08/799,793	2/12/1997	INTEGRATED CIRCUIT WITH THIN FILM RESISTORS AND A METHOD FOR CO-PATTERNING THIN FILM RESISTORS WITH DIFFERENT COMPOSITIONS
09/335,134	6/17/1999	INTEGRATED CIRCUIT WITH THIN FILM RESISTORS AND A METHOD FOR CO-PATTERNING THIN FILM RESISTORS WITH DIFFERENT COMPOSITIONS
08/671,453	6/27/1996	SILENT START CLASS D AMPLIFIER
08/707,271	9/3/1996	P-COLLECTOR HV PMS SWITCH VT ADJUSTED SOURCE/DRAIN
08/671,157	6/28/1996	DOUBLE DIFFUSED MOS DEVICE AND METHOD
08/726,659	10/7/1996	SURFACE MOUNT DIE BY HANDLE REPLACEMENT
09/110,721	7/7/1998	SURFACE MOUNT DIE BY HANDLE REPLACEMENT
08/066,355	5/21/1993	INTEGRATED CIRCUIT METHOD FOR AND STRUCTURE WITH NARROW LINE WIDTHS
08/460,993	6/5/1995	INTEGRATED CIRCUIT METHOD FOR AND STRUCTURE WITH NARROW LINE WIDTHS
08/292,482	8/18/1994	LOW NOISE LOGIC FAMILY
08/125,411	9/22/1993	DIE SEPARATION METHOD FOR SILICON ON DIAMOND CIRCUIT STRUCTURES
08/108,358	8/18/1993	SUB-MICRON BONDED SOI BY TRENCH PLANARIZATION
07/785,395	10/30/1991	ANALOG-TO-DIGITAL CONVERTER AND METHOD OF FABRICATION
08/287,763	8/9/1994	ANALOG-TO-DIGITAL CONVERTER AND METHOD OF FABRICATION
92/09,66	10/29/1992	ANALOG-TO-DIGITAL CONVERTER AND METHOD OF FABRICATION
08/438,251	5/10/1995	MULTI-CHANNEL SIGMA-DELTA A/D CONVERTERS WITH IMPROVED THROUGHPUT
08/292,588	8/18/1994	TRENCH INSOLATION STRESS RELIEF
08/465,246	6/5/1995	TRENCH INSOLATION STRESS RELIEF
08/248,844	5/25/1994	SILICON ON DIAMOND CIRCUIT STRUCTURE
08/513,950	12/4/1995	BONDED WAFER PROCESS INCORPORATING DIAMOND INSULATOR
08/783,792	1/15/1997	BONDED WAFER PROCESSING
08/843,302	4/14/1997	BONDED WAFER PROCESSING
08/430,312	4/28/1995	BONDED WAFER PROCESSING
08/137,293	10/14/1993	BONDED WAFER PROCESSING
07/917,635	7/20/1992	ANALOG-TO-DIGITAL CONVERTER AND METHOD OF FABRICATION
08/391,490	2/21/1995	ANALOG-TO-DIGITAL CONVERTER AND METHOD OF FABRICATION
07/984,187	11/20/1992	ANALOG-TO-DIGITAL CONVERTER AND METHOD OF FABRICATION
08/956,074	10/22/1997	ANALOG-TO-DIGITAL CONVERTER AND METHOD OF FABRICATION
08/733,368	10/17/1996	LATE PROCESS METHOD AND APPARATUS FOR TRENCH ISOLATION
08/745,104	11/7/1996	LATE PROCESS METHOD AND APPARATUS FOR TRENCH ISOLATION
08/741,639	10/28/1996	CAPACITOR STRUCTURE IN A BONDED WAFER AND METHOD OF FABRICATION
08/305,366	9/13/1994	CONSTANT DELAY LOGIC CIRCUITS AND METHODS
08/331,015	10/28/1994	SIGMA-DELTA ANALOG TO DIGITAL CONVERTER WITH THREE POINT CALIBRATION APPARATUS AND METHOD
08/490,566	6/15/1995	EFFICIENT BATTERY OPERATED INVERTER CIRCUIT FOR CAPACITIVE LOADS SUCH AS ELECTROLUMINESCENT LAMPS
08/490,016	6/13/1995	BATTERY OPERATED INVERTER CIRCUIT FOR CAPACITIVE LOADS SUCH AS ELECTROLUMINESCENT LAMPS
08/490,952	6/13/1995	ELECTROLUMINESCENT LAMP DRIVER SYSTEM
08/461,643	6/5/1995	SURFACE MOUNTABLE INTEGRATED CIRCUIT WITH CONDUCTIVE VIAS
07/921,197	7/28/1992	BONDED WAFER PROCESSING
08/287,773	8/9/1994	BONDED WAFER PROCESSING
08/573,551	12/15/1995	BONDED WAFER PROCESSING
08/299,741	9/1/1994	HIGH SPEED COMPARATOR
08/180,666	1/13/1994	VOLTAGE INDEPENDENT SYMMETRICAL CURRENT SOURCE
07/935,765	8/26/1992	METHOD FOR FORMING RECESSED OXIDE INSOLATION CONTAINING DEEP AND SHALLOW TRENCHES
08/339,966	11/15/1994	METHOD FOR FORMING RECESSED OXIDE INSOLATION CONTAINING DEEP AND SHALLOW TRENCHES
07/785,325	10/30/1991	ANALOG-TO-DIGITAL CONVERTER AND METHOD OF FABRICATION
08/645,139	5/13/1996	ANALOG-TO DIGITAL CONVERTER AND METHOD OF FABRICATION
08/571,693	12/31/1995	ANALOG-TO-DIGITAL CONVERTER AND METHOD OF FABRICATION
08/630,874	4/2/1996	ANALOG-TO-DIGITAL CONVERTER AND METHOD OF FABRICATION
08/739,898	10/30/1996	ANALOG-TO-DIGITAL CONVERTER AND METHOD OF FABRICATION
09/394,802	9/10/1999	ANALOG-TO-DIGITAL CONVERTER AND METHOD OF FABRICATION
08/885,707	6/30/1997	METHOD FOR FORMING COMPLIMENTARY WELLS AND SELF-ALIGNED TRENCH WITH A SINGLE MASK
08/885,707	6/30/1997	METHOD FOR FORMING COMPLIMENTARY WELLS AND SELF-ALIGNED TRENCH WITH A SINGLE MASK
09/345,266	6/30/1999	METHOD FOR FORMING COMPLIMENTARY WELLS AND SELF-ALIGNED

		TRENCH WITH A SINGLE MASK
08/884,726	6/30/1997	SELF-ALIGNED POWER MOSFET IN SILICON CARBIDE
07/133,902	3/25/1980	POWER MOSFET WITH AN ANODE REGION
08/975,472	11/21/1997	POWER MOSFET WITH AN ANODE REGION
08/654,316	5/28/1996	SEMICONDUCTOR PACKAGING APPARATUS AND METHOD
09/204,904	12/3/1998	SEMICONDUCTOR PACKAGING APPARATUS AND METHOD
09/014,844	1/28/1998	FOR BRUSHLESS DC MOTOR PWM SCHEME FOR QUIET COMMUTATION
09/062,964	4/20/1998	DEVICES WITH AND METHODS FOR PATTERNED WELLS
09/082,892	5/21/1998	DEFECT GATHERING BY INDUCED STRESS
09/334,987	6/17/1999	DEFECT GATHERING BY INDUCED STRESS
09/123,975	7/29/1998	COMPACT TRANSMISSION LINES
09/129,321	8/5/1998	A LOW POWER DISCRETE SEMICONDUCTOR SURFACE MOUNT PACKAGING DESIGN
09/139,932	8/26/1998	PARASITIC CURRENT BARRIERS
09/183,453	10/30/1998	OVERCURRENT SENSING CIRCUIT AND SELF ADJUSTING BLANKING
09/173,111	10/15/1998	A VARIABLE FREQUENCY CLASS D MODULATOR WITH BUILT IN SOFT CLIPPING AND FREQUENCY LIMITING
09/183,879	11/18/1998	CLASS D MODULATOR WITH DIGITAL CURRENT LIMIT AND LOAD IMPEDANCE SENSING CIRCUITS
09/183,879	10/30/1998	START-UP CIRCUIT FOR SELF OSCILLATING CLASS D MODULATOR
09/150,429	09/09/1998	DEVICE CONTAINING SAMPLE PREPARATION SITES FOR TRANSMISSION ELECTRON MICROSCOPIC ANALYSIS AND PROCESSES OF FORMATION AND USE
09/166,416	10/5/1998	SEMICONDUCTOR INTEGRATED CIRCUIT WITH TEMPORARILY INTERCONNECTED BOND PADS
09/358,625	7/21/1999	DOUBLY GRADED JUNCTION TERMINATION EXTENSION (JTE) FOR EDGE PASSIVATION OF SEMICONDUCTOR DEVICES
09/307,879	5/10/1999	PROCESS FOR FORMING MOS-GATED DEVICES HAVING SELF-ALIGNED TRENCHES
09/324,553	6/3/1999	LOW VOLTAGE DUAL-WELL MOS TECHNOLOGY FOR ACHIEVING HIGH RUGGEDNESS LOWER ON-RESISTANCE AND LOWER REVERSE RECOVERED CHARGE
09/334,835	6/17/1999	SELF-SUPPORTED ULTRATHIN SILICON WAFER PROCESS
09/450,872	11/29/1999	EMITTER BALLAST RESISTOR WITH ENHANCED BODY EFFECT TO IMPROVE TH SHORT CIRCUIT WITHSTAND CAPABILITY OF POWER DEVICES
09/428,616	10/27/1999	TECHNIQUE FOR MINIMIZING GATE CHARGE AND GATE TO DRAIN CAPACITANCE IN POWER MOS DEVICES SUCH AS DMOS, IGBTS AND MOSFETS
09/339,356	6/24/1999	BACKMETAL DRAIN TERMINAL WITH LOW STRESS AND THERMAL RESISTANCE
09/260,411	3/1/1999	SELF-ALIGNED HIGH DENSITY TRENCH GATED DEVICE
09/342,948	6/29/1999	BRUSHLESS MULTIPASS SILICON WAFER CLEANING PROCESS FOR POST CHEMICAL MECHANICAL POLISHING USING IMMERSION
09/307,896	5/10/1999	LASER DECAPSULATION OF SEMICONDUCTOR DEVICES
09/255,231	2/22/1999	METHOD FOR FORMING A BONDED SUBSTRATE CONTAINING A PLANAR INTRINSIC GATHERING ZONE AND SUBSTRATE FORMED BY SAID METHOD
09/303,270	4/30/1999	POWER MOS DEVICE WITH INCREASED CHANNEL WIDTH AND PROCESS FOR FORMING SAME
09/283,536	4/1/1999	IMPROVED POWER TRENCH MOST GATED TRANSISTOR
09/283,531	4/1/1999	METHOD OF MAKING HIGH DENSITY POWER TRENCH MOS-GATED TRANSISTOR
09/358,266	7/21/1999	USE OF A BARRIER REFRACTIVE OR ANTI-REFLECTIVE LAYER AND DIELELECTRIC LAYER TO IMPROVE THE LASER TRIM CHARACTERISTICS OF A LASER TRIMMED THIN FILM RESISTOR
09/339,274	6/23/1999	INTEGRATED RESISTIVE CONTRACT
09/343,845	6/30/1999	IMPROVED SOLDERABILITY OF PLATED ELECTRONIC TERMINATIONS
09/345,261	6/30/1999	METHOD FOR MAKING A DIFFUSED BACK-SIDE LAYER ON A BONDED - WAFER WITH A THICK BOND OXIDE
09/350,575	7/9/1999	IMPROVED DENSE MCT USING SELF-ALIGNED SILICIDATION WITH COMPLEX SPACERS
09/318,334	5/25/1999	TRENCH-GATED DEVICE HAVING TRENCH WALLS FORMED BY SELECTIVE EPITAXIAL GROWTH AND PROCESS FOR FORMING DEVICE
09/344,856	6/28/1999	A NOVEL METHOD OF FILM ETCH/REMOVAL VERIFICATION IN AN IN-SITU ETCH AND DEPOSITION
09/314,323	5/19/1999	MOS GATED POWER DEVICE HAVING EXTENDED TRENCH AND DOPING ZONE AND PROCESS FOR FORMING SAME
09/345,930	7/1/1999	POWER SEMICONDUCTOR MOUNTING PACKAGE CONTAINING BALL GRID ARRAY
09/344,867	6/28/1999	POTTED TRANSDUCER ARRAY WITH MATCHING NETWORK IN A TWO OR MORE PASS CONFIGURATION
09/344,868	6/28/1999	EDGE TERMINATION FOR SILICON DEVICES
09/345,929	7/1/1999	LOW TEMPERATURE COEFFICIENT RESISTOR (TCRL)
09/342,376	6/29/1999	DUAL MODE CLASS D AMPLIFIERS

09/367,325	8/11/1999	CO-PATTERNING THIN FILM RESISTORS OF DIFFERENT COMPOSITIONS WITH A CONDUCTIVE HARD MASK AND METHOD FOR SAME
09/437,678	11/10/1999	LOW NOSIE LOW DISTORTION CLASS D AMPLIFIER
09/437,393	11/10/1999	CLASS D AMPLIFIER WITH BANDWIDTH INDEPENDENT OF LOAD IMPEDANCE
09/438,210	11/12/1999	CLASS D MODULATOR WITH PEAK CURRENT LIMIT AND LOAD IMPEDANCE SENSING CIRCUITS
09/442,291	11/19/1999	BACKWARDS DRIVABLE MOS OUTPUT DRIVER